REMARKS

The final Office Action of October 6, 2006, has been received and reviewed.

Claims 1-14 are currently pending and under consideration in the above-referenced application, each standing rejected.

New claim 15 has been added.

Reconsideration of the above-referenced application is respectfully requested.

Supplemental Information Disclosure Statement

Please note that a Supplemental Information Disclosure Statement was filed in the above-referenced application on October 3, 2006, but that the undersigned attorney has not yet received any indication that the references cited in the Supplemental Information Disclosure Statement have been considered in the above-referenced application. It is respectfully requested that the reference cited in the Supplemental Information Disclosure Statement of October 3, 2006, be considered and made of record in the above-referenced application and that an initialed copy of the Form PTO/SB/08A that accompanied that Supplemental Information Disclosure Statement be returned to the undersigned attorney as evidence of such consideration.

Rejections under 35 U.S.C. § 103(a)

Claims 1-14 stand rejected under 35 U.S.C. § 103(a).

The standard for establishing and maintaining a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Saka in View of Sahota

Claims 1-14 stand rejected under 35 U.S.C. § 103(a) for being drawn to subject matter that is allegedly unpatentable over the subject matter taught in U.S. Patent 6,476,921 to Saka et al. (hereinafter "Saka"), in view of teachings from U.S. Patent 5,665,199 to Sahota et al. (hereinafter "Sahota").

Saka teaches a system that uses reflectance to analyze a wafer during polishing and selectively applies different amounts of pressure to the same wafer in response to the analyzed reflectance to improve the planarity of a polished surface of the wafer. *See, e.g.,* Abstract; FIG. 4; col. 7, lines 14-56. Data obtained from such analysis may also be used to generate a pressure profile for application substrates that are subsequently polished. Col. 8, lines 27-35.

The Advisory Action of December 21, 2006, provides, "Saka et al fails to [teach] topography as the basis of analysis." The Office has relied on Sahota for this teaching. Specifically, it has been asserted that Sahota "teaches analysis of the topography of a wafer to determine progress of polishing . . ." Advisory Action of December 21, 2006. Sahota teaches that a "film coating thickness at . . . four locations on [a] first patterned test wafer" may be measured to develop polishing processes that are tailored for use in polishing specific types of material films over specific types of semiconductor device structures. *See* col. 2, lines 33-36. One of these measured locations is "a first position over a measurable topographic feature . . ." col. 2, lines 15-16; *see also,* col. 17, lines 64-67.

It is respectfully submitted that measuring a film thickness over a "measurable topographic feature" does not amount to "analyzing a topography of an active surface." It is further submitted that Sahota lacks any teaching or suggestion as to analyzing the topography of a wafer.

As neither Sato nor Sahota teaches or suggests "analyzing a topography of an active surface," it is respectfully submitted that the teachings of these references cannot be relied upon to establish a *prima facie* case of obviousness against independent claim 1 or independent claim 8. Therefore, it is respectfully submitted that, under 35 U.S.C. § 103(a), the subject matter

to which independent claims 1 and 8 are directed is allowable over the subject matter taught in Sato and Sahota.

Claims 2-7 and 13 are each allowable, among other reasons, for depending directly or indirectly from independent claim 1, which is allowable.

Each of claims 9-12 and 14 is allowable, among other reasons, for depending directly from independent claim 8, which is allowable.

Nagahara in View of Sahota

Claims 1-14 are also rejected under 35 U.S.C. § 103(a) for being drawn to subject matter that is allegedly unpatentable over the subject matter taught in U.S. Patent 6,351,397 to Nagahara et al. (hereinafter "Nagahara"), in view of teachings from Sahota.

The teachings of Nagahara relate to a wafer carrier assembly 204 for use with a polishing apparatus. The wafer carrier assembly 204 includes a wafer carrier 206, which is configured to receive a backside 217 of a wafer 212. Col. 5, lines 29-31; FIG. 2a. A plurality of air lines 236a, 236b, 236c establish communication between air sources 234a, 234b, 234c and the wafer carrier 206. Col. 5, lines 45-50; FIG. 2a. A negative pressure may be applied to a central region of the backside 217 of the wafer 212 by one air line 236a to hold the wafer 212 in place within the wafer carrier 206. Col. 5, line 58, to col. 6, line 20 (*see* col. 6, lines 4 and 5, specifically); FIG. 2a. Other air lines 236b, 236c may be used to apply positive pressure to different locations on the backside 217 of the wafer 212. Col. 5, line 58, to col. 6, line 20; FIG. 2a. The application of different amounts of air pressure to different locations on the backside 217 of the wafer 212 distorts the wafer 212 in a desired manner. *See, e.g.,* col. 5, line 65, to col. 6, line 2.

It does not appear that the wafer carrier 206 is configured to isolate pressures that are communicated thereto and applied to the backside 217 of the wafer 212, nor does Nagahara teach or suggest that such isolation may occur. Thus, it appears that any pressures that are applied to the backside 217 of a wafer 212 would be evenly distributed, or at least distributed as gradients, rather than as discrete amounts of pressure.

The teachings of Sahota are summarized above.

It is respectfully submitted that neither Nagahara nor Sahota teaches or suggests analyzing a topography of an active surface, as is required by both independent claim 1 and independent claim 8.

In addition to analyzing the topography of a surface of a first polished semiconductor device structure, the method of independent claim 8 includes selectively applying distinctly increased amounts of pressure to at least two locations on the backside of at least one second semiconductor device structure, relative to pressure applied to immediately adjacent areas, with the at least two locations corresponding to raised areas on an active surface of the first semiconductor device structure. The active surface of the at least one second semiconductor device structure is polished as the pressure is applied to the backside thereof.

It is respectfully submitted that Nagahara and Sahota both lack any teaching or suggestion of selectively applying distinctly increased amounts of pressure, relative to immediately adjacent areas of a semiconductor device structure, to at least two locations on a backside of the semiconductor device structure. Nagahara teaches that air pressure may be applied to a wafer carrier 206, but lacks any teaching or suggestion that the applied air pressure is confined. As such, it would be spread out, resulting in the application of pressure at one location that is not distinctly increased relative to pressure applied at immediately adjacent locations. Sahota also lacks any teaching or suggestion that different amounts of pressure may be applied to different locations of a semiconductor device structure.

Since Nagahara and Sahota do not teach or suggest each and every element of independent claim 1 or independent claim 8, it is respectfully submitted that the teachings of these references do not support a *prima facie* case of obviousness against independent claim 1 or independent claim 8. It is, therefore, respectfully submitted that, under 35 U.S.C. § 103(a), independent claims 1 and 8 are both directed to subject matter that is allowable over the subject matter taught in Nagahara and Sahota.

Claims 2-7 are each allowable, among other reasons, for depending directly or indirectly from independent claim 1, which is allowable.

Each of claims 9-12 and 14 is allowable, among other reasons, for depending directly from independent claim 8, which is allowable.

Korovin in View of Sahota

Claims 1-14 have also been rejected under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly unpatentable over the teachings of U.S. Patent 6,390,905 to Korovin et al. (hereinafter "Korovin"), in view of teachings from Sahota.

The apparatus of Korovin includes a web diaphragm 100 with a plurality of ribs 101-104. FIG. 1; col. 5, lines 54-56. In the embodiment of the apparatus shown in FIG. 1, each rib 101-104 includes a bottom edge that is configured to contact a backside of a semiconductor wafer 150. Col. 7, lines 20-24. The ribs 101-104 act as the barriers between adjacent web plenums 111-114. Col. 6, lines 10-14. Each web plenum 111-114 is configured to receive and contain pressurized fluid, which exerts pressure upon an area on the backside of the wafer 150. Col. 6, lines 53-56. Different amounts of pressure may be applied to areas of the backside that communicate with different web plenums 111-114.

The relevant teachings of Sahota are summarized above.

It is respectfully submitted that one of ordinary skill in the art wouldn't have been motivated to combine teachings from Korovin with teachings from Sahota. Korovin teaches a method for counteracting visible bulges that are present in incoming wafers (*see, e.g.,* FIG. 10), whereas Sahota teaches a process that includes measuring a material layer thickness at a small number of precise locations on a semiconductor device structure. One of ordinary skill in the art would expect increased polishing of bulges to decrease the overall thickness uniformity of the polished layer, which is contrary to the stated purpose of the process disclosed in Sahota: to develop a polishing process that "results in a controlled, uniform, and reproducible ILD [interlayer dielectric] thickness." Col. 1, lines 55-59. As such, it is respectfully submitted that one of ordinary skill in the art wouldn't have been motivated to combine teachings from Korovin and Sahota in the manner that has been asserted.

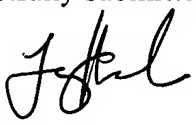
New Claim

New claim 15 depends from independent claim 1 and includes elements that have been removed from independent claim 1. It is respectfully submitted that new claim 15 does not introduce new matter into the above-referenced application. Moreover, it is submitted that new claim 15 is allowable, among other reasons, for depending from independent claim 1, which is allowable.

CONCLUSION

It is respectfully submitted that each of claims 1-15 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



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Date: February 6, 2007
BGP:TH/dn:eg
Document in ProLaw